in real mode, the original PC-AT IBM used the free lines of the keyboard controller to command the line A20. The keyboard controller invalidates the line A20 when the processor is running in real mode, to keep the compatibility with the precedent PCs and validates it when passing to protected mode. Microsoft developed a special driver, HIMEM.SYS, which allows the line A20 to be manipulated under soft control, allowing access to HMA in real mode. By practical reasons, HMA is normally used by the DOS system to keep a part of its code, emptying approximately 45Kbytes of RAM from the conventional memory. This can be done by specifying in CONFIG.SYS "DOS=HIGH".

11.2.4 Extended Memory (XMS) represents the memory above 1MB, that is the addressability limit for the original 8088 PCs processor. Except the HMA area, the extended memory is not accessible to a PC running in real mode. There are two ways to use the extended memory: the system may operate in fully protected mode like Windows NT and it can access directly the extended memory, or the other way, used by other operating systems or applications running in real mode (including DOS programs that need access to the extended memory). Windows 3.x and Windows 95 must coordinate their access using an extended memory manager. The most popular manager is HIMEM.SYS, in agreement with the extended memory (XMS) user specifications.

11.3 Applications

The presented application is connecting a 4Kbytes EPROM memory and a 16Kbytes SRAM memory in a PC system, in the empty places of the extension slots. The start address of the EPROM memory is considered to be CC000h and for the SRAM memory – D0000h (see fig.11.5)

11.3.1 Connecting EPROM memories to the system

Two circuits I2716, EPROM memories of 2Kbytes were used. Figure 11.6 presents the circuit and its pins assignment. The main problem in connecting a memory or a port to the system is the decoder circuit, which allows addressing in the desired or authorized address area. The memory address decoder must be conceived depending on the memory start address and the memory dimensions. In this case, a 4Kbytes memory is connected starting from the address CC000h.

The number of address lines necessary to decode the memory block will be computed. For 1Kbytes=2^{10} we need 10 address lines. For 2Kbytes=2*1Kbytes we need 11 lines, and for 4Kbytes – 12 lines.

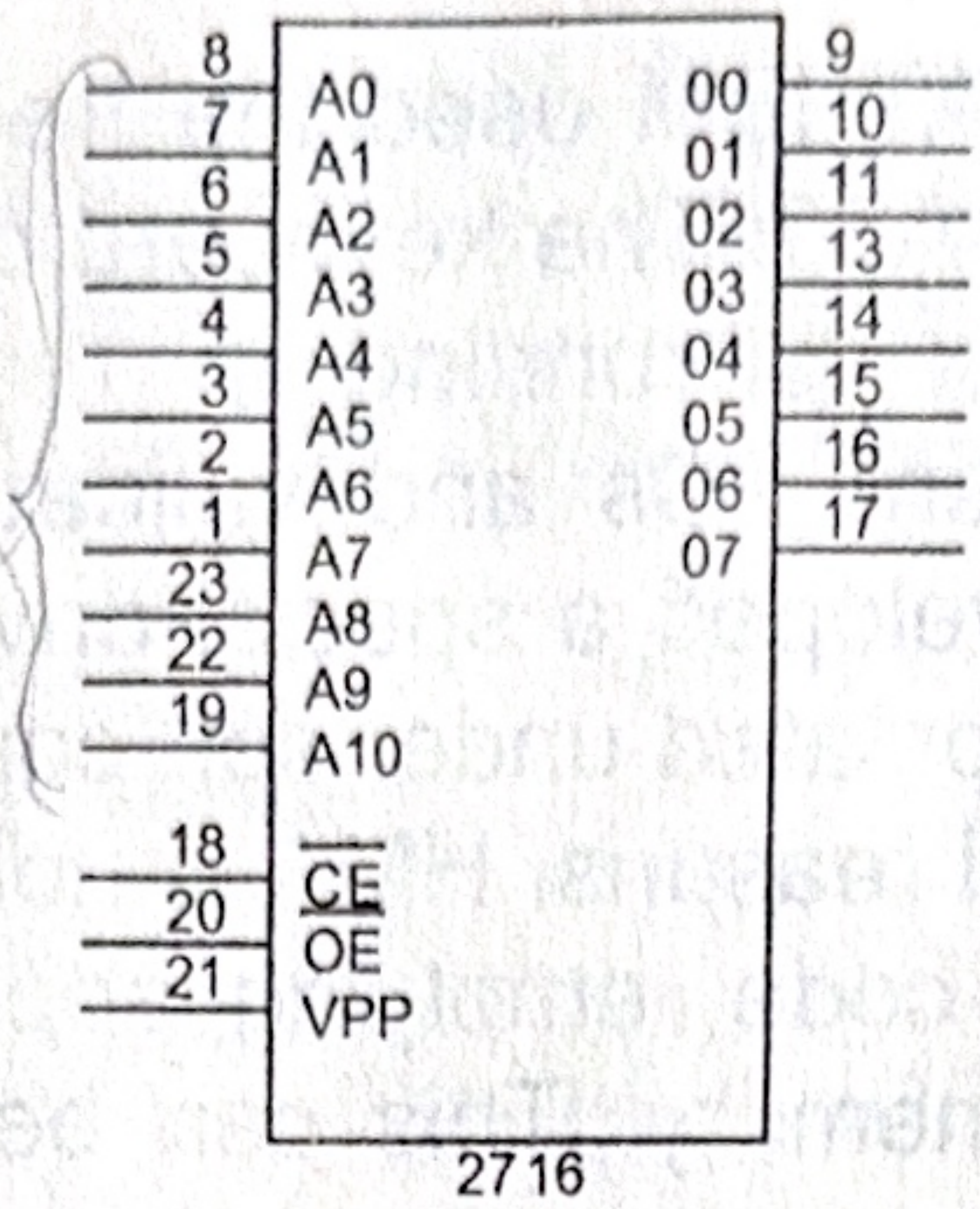

Fig.11.6 EPROM memory pins assignment (2Kbytes)

A0-A10 = address lines
D0–D7 = data lines
/CE = memory selection signal, active on "0" ("chip enable")
/OE = memory read validation signal, active on "0" ("output enable")
V_{pp} = voltage that allows data writing to memory if 25V is applied

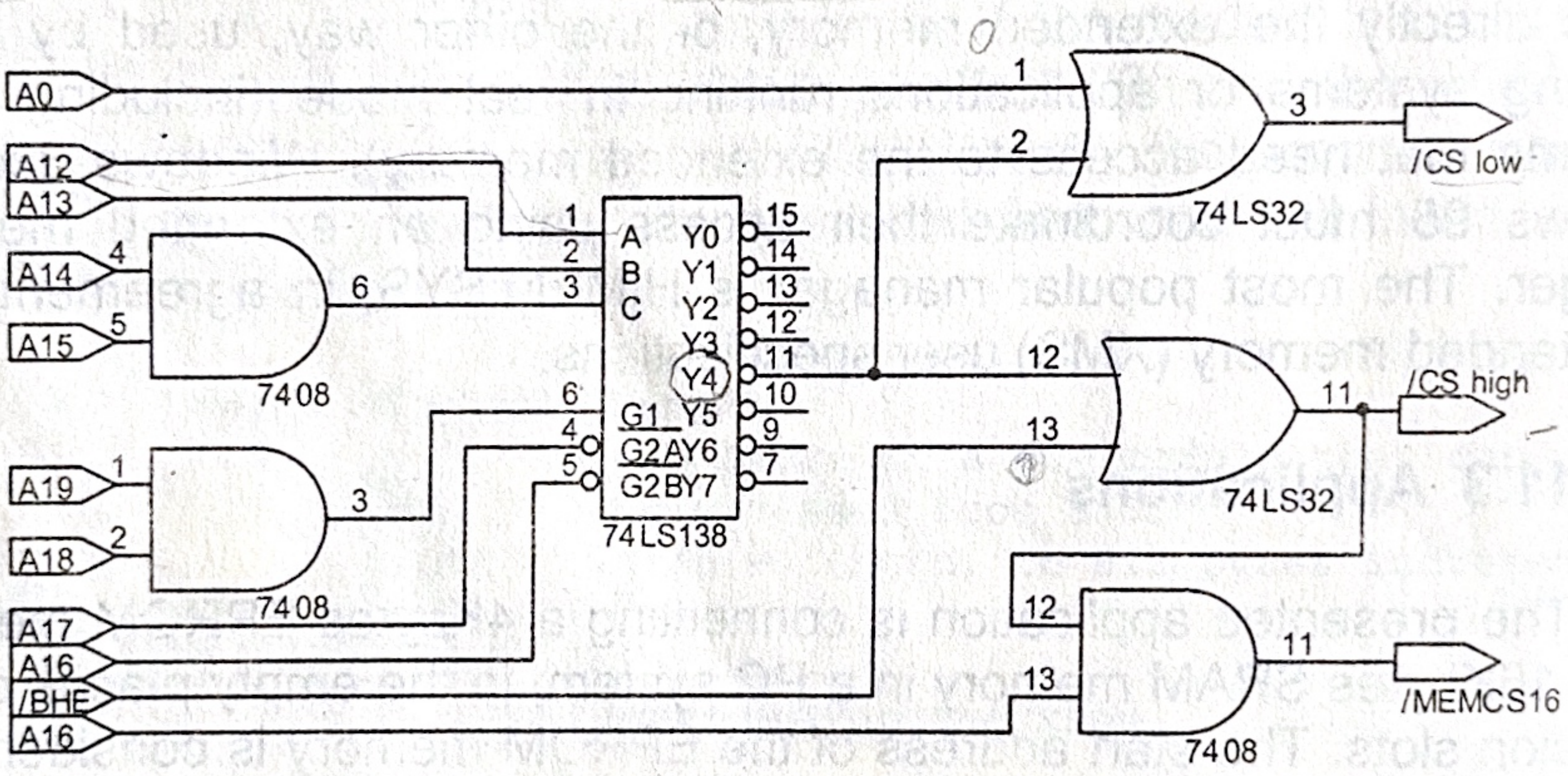

Fig.11.7 The address decoder for the EPROM memories

In table 11.2 the address lines used by the decoder and for addressing the memory are presented.

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
1	1	0	0	1	1	0	0	x	x
A9	**A8**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
X	X	X	X	X	X	X	X	X	A0

Table 11.2 EPROM decoder address lines

The address lines A19-A12 are used in both memory banks, and lines A11-A1 will be used for addressing. A0 is used in selecting the low (even) bank if A0="0" or the high (odd) one if A0="1" and /BHE="0". Figure 11.7 presents the decoder made according to the table 11.2.

11.3.2 Connecting SRAM memories to the system

Two 6264 circuits were used, 8Kbytes SRAM memories. Figure 11.10 presents the circuit. Just like for the EPROM circuit, to read/write from/to the memory, we need an address decoder. The start address is D0000h and the address lines to generate CS2 and the lines for addressing are determined in the same way as before.

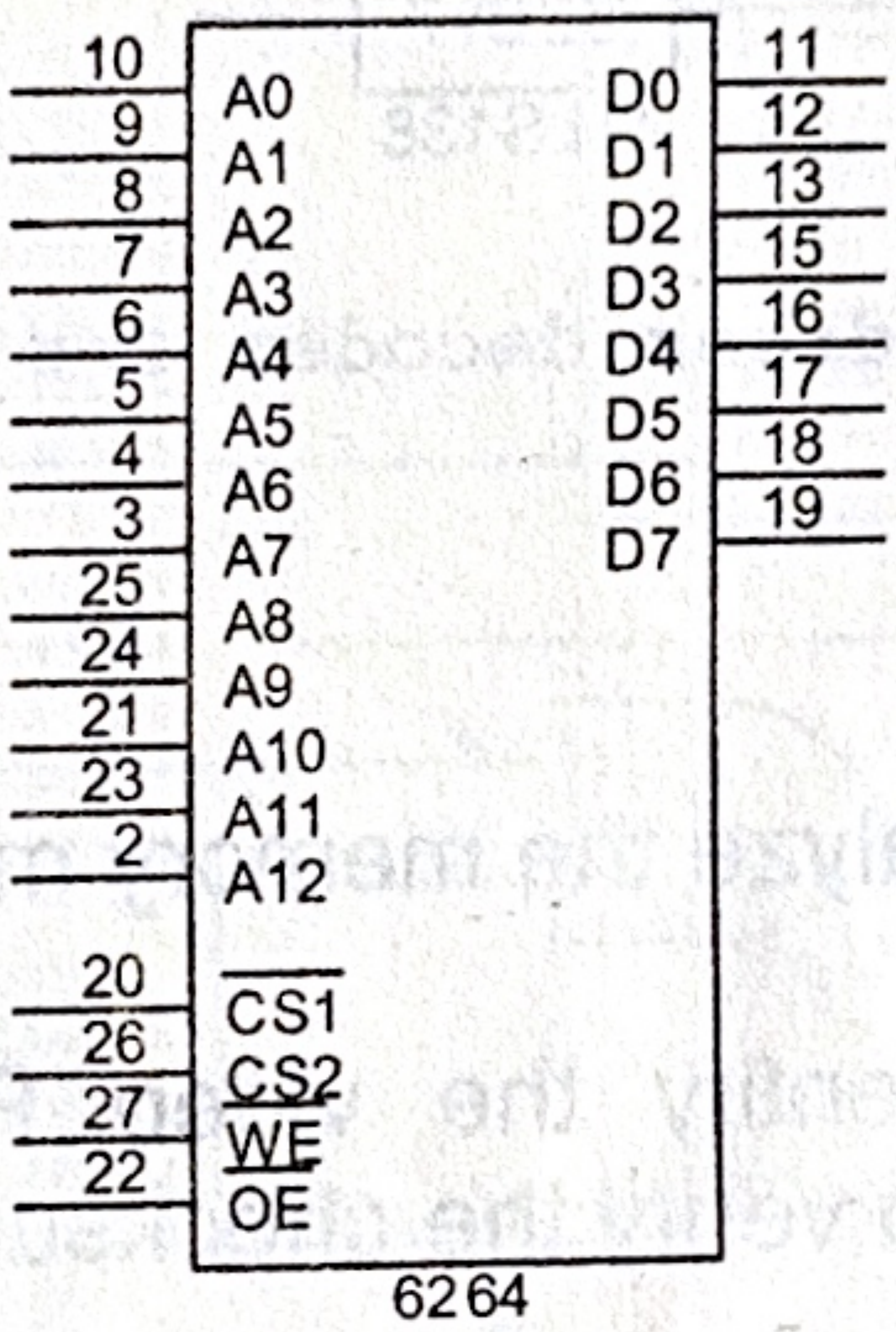

Fig.11.8 SRAM memory pins assignment (8 Kbytes)

A0-A12 = address lines
D0 –D7 = data lines
/CS1 = memory selection signal, active on "0" ("Chip select")
CS2 = memory selection signal, active on "1" ("Chip select")
/WE = memory write command signal, active on "0"("Write enable")
/OE = memory read validation signal, active on "1" ("output enable")

The table 11.3 is used for designing the address decoder.

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
1	1	0	1	0	0	x	x	x	x
A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
X	X	X	X	X	X	X	X	X	A0

Table 11.3 SRAM decoder address lines

The lines A19-A14 will be used to generate the signal CS2 and A13-A1 will be used to address the memory. A0 is used to select the low (even) memory bank, because it is connected to /CS1 from a memory circuit and /BHE is connected to /CS1 from the other memory, to select the high (odd) memory bank.

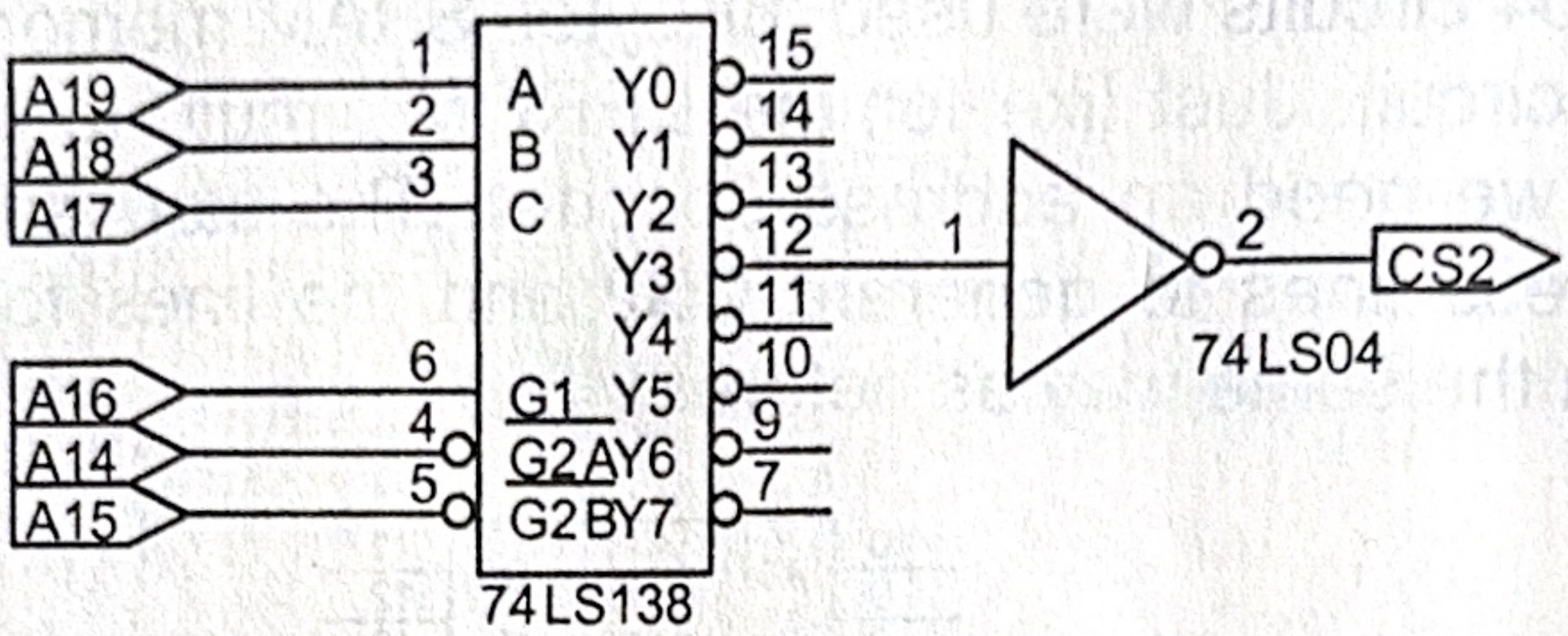

Fig.11.9 The address decoder for the SRAM memories

11.4 Exercise

a. Using CHECKIT, analyze the memory map on the workstation.

b. Using SDEBUG, identify the video ROM signature and write a program sequence to verify the checksum.

c. Analyze the connection of the memories to the ISA bus, presented in the appendix. What is the role of MEMCS16? Suggest a schematic that uses only one decoder circuit for EPROM and RAM.

d. Using CHECKIT detect the memories connected to the system on the ISA bus and analyze the EPROMs contents.

e. Write an application for detecting the ROM blocks from the memory map.

f. Write a program in assembling language that makes a self-copy in UMA (SRAM) and launches itself.

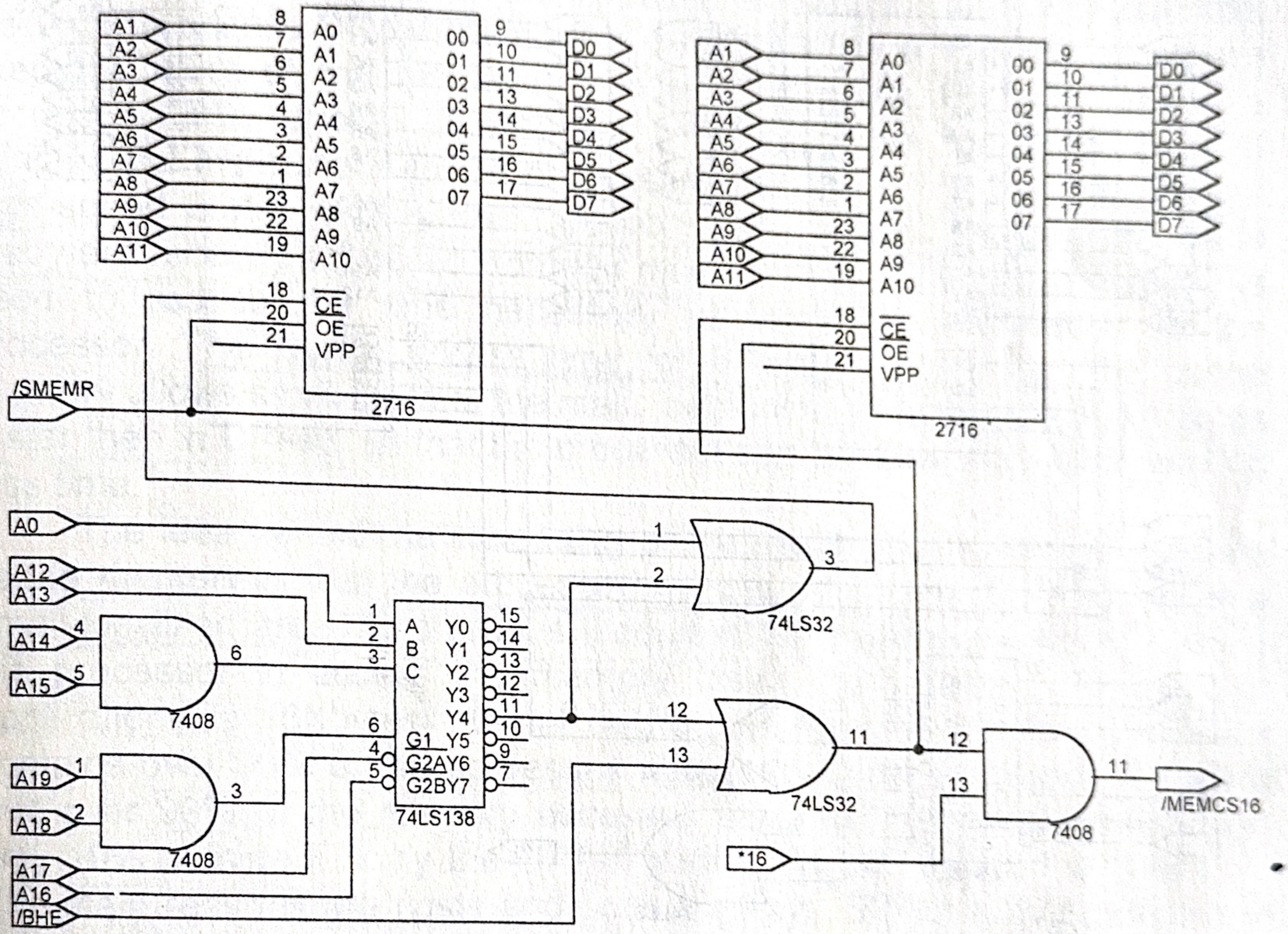

Fig.11.10 Electrical schematic for the EPROM memories block

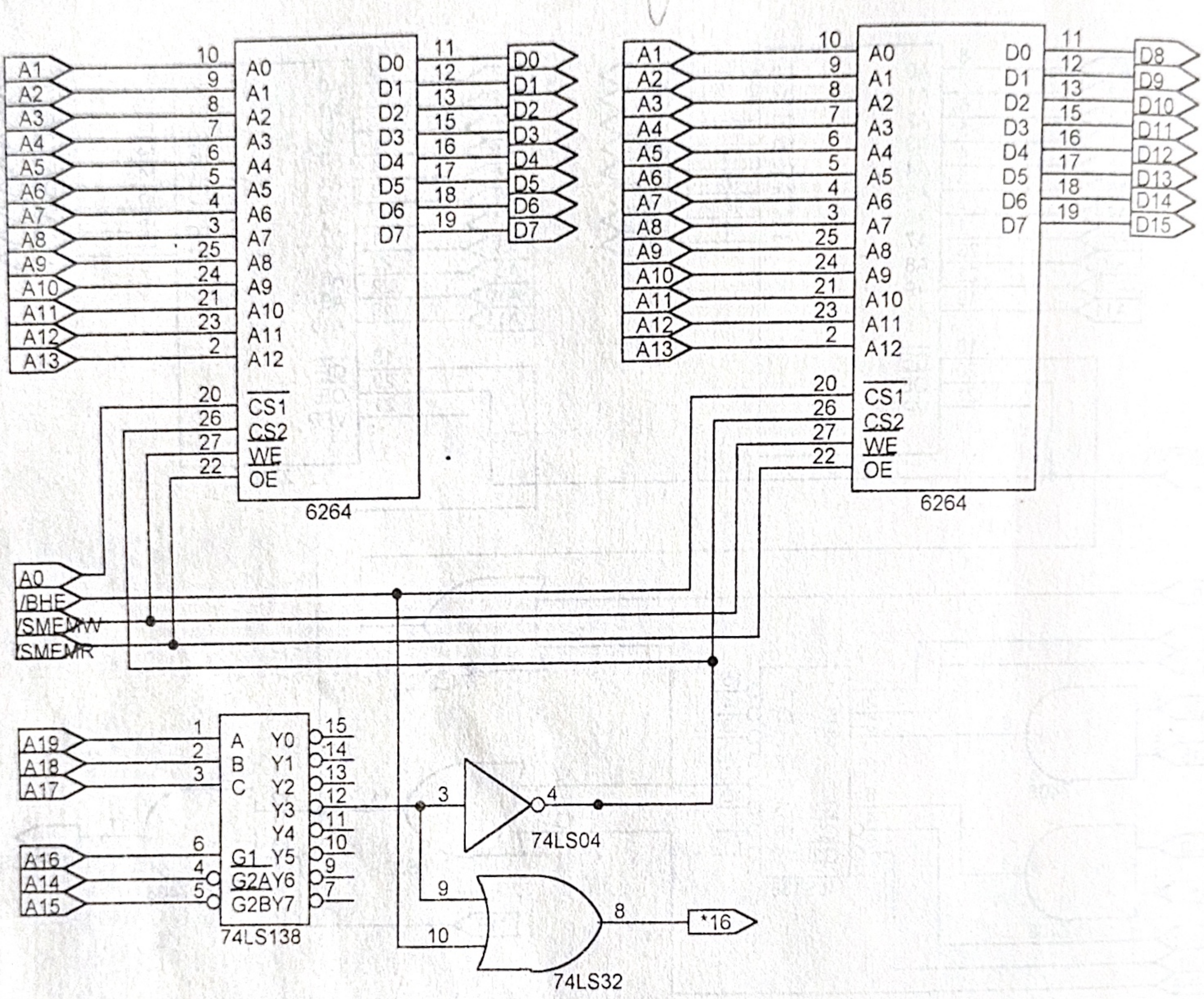

Fig.11.11 Electrical schematic for the SRAM memories block